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Kikkawa

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(54) **COMPOUND SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD OF THE SAME**

(71) Applicant: **Transphorm Japan, Inc.**, Yokohama, Kanagawa (JP)

(72) Inventor: **Toshihide Kikkawa**, Machida (JP)

(73) Assignee: **Transphorm Japan, Inc.**, Yokohama (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **14/561,450**

(22) Filed: **Dec. 5, 2014**

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US 2015/0078038 A1 Mar. 19, 2015

Related U.S. Application Data

(63) Continuation of application No. 13/787,788, filed on Mar. 6, 2013, now Pat. No. 8,933,489.

(30) **Foreign Application Priority Data**

Mar. 29, 2012 (JP) 2012-077624

(51) **Int. Cl.**
H01L 29/205 (2006.01)
H01L 29/778 (2006.01)
(Continued)

(52) **U.S. Cl.**
CPC ***H01L 29/7787*** (2013.01); ***H01L 21/0254*** (2013.01); ***H01L 21/02458*** (2013.01); ***H01L 21/02518*** (2013.01); ***H01L 29/201*** (2013.01);
(Continued)

(58) **Field of Classification Search**
CPC H01L 29/1083; H01L 29/778–29/7801; H01L 29/66462; H01L 21/26533; H01L 29/201; H01L 29/205; H01L 29/207; H01L 29/2003; H01L 29/7787
USPC 438/167, 172, 602, 604–606; 257/11, 257/200, 615, 745
See application file for complete search history.

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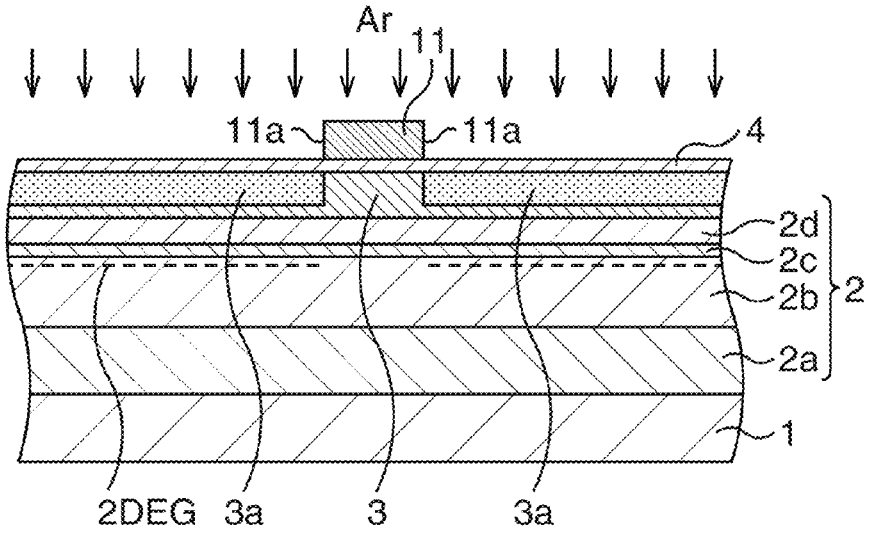
Primary Examiner — Laura Menz
Assistant Examiner — Maliheh Malek
(74) *Attorney, Agent, or Firm* — Fish & Richardson P.C.

(57) **ABSTRACT**

An AlGaN/GaN.HEMT includes, a compound semiconductor lamination structure; a p-type semiconductor layer formed on the compound semiconductor lamination structure; and a gate electrode formed on the p-type semiconductor layer, in which Mg being an inert element of p-GaN is introduced into both sides of the gate electrode at the p-type semiconductor layer, and introduced portions of Mg are inactivated.

20 Claims, 11 Drawing Sheets



(51) **Int. Cl.**

H01L 21/02	(2006.01)
H02M 3/335	(2006.01)
H01L 29/66	(2006.01)
H01L 29/20	(2006.01)
H01L 29/207	(2006.01)
H01L 29/201	(2006.01)
H02M 1/088	(2006.01)
H01L 29/10	(2006.01)

(52) **U.S. Cl.**

CPC ***H01L 29/2003*** (2013.01); ***H01L 29/205*** (2013.01); ***H01L 29/207*** (2013.01); ***H01L 29/66462*** (2013.01); ***H01L 29/778*** (2013.01); ***H02M 1/088*** (2013.01); ***H02M 3/33507*** (2013.01); ***H02M 3/33569*** (2013.01); *H01L 21/0262* (2013.01); *H01L 21/02576* (2013.01); *H01L 21/02579* (2013.01); *H01L 29/1066* (2013.01)

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FIG. 1A

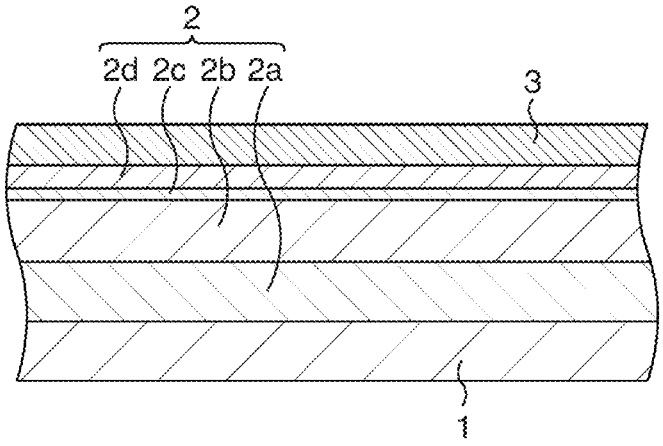


FIG. 1B

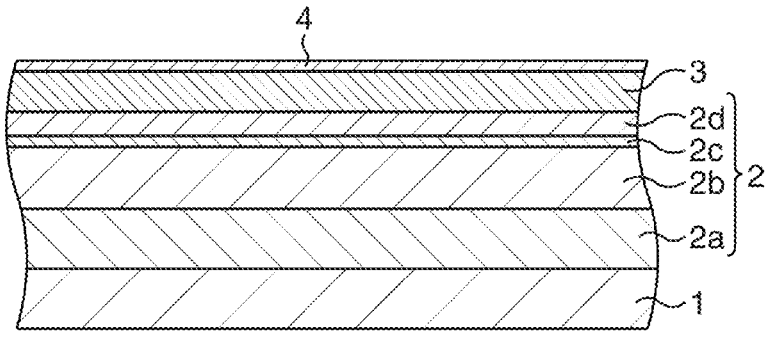


FIG. 1C

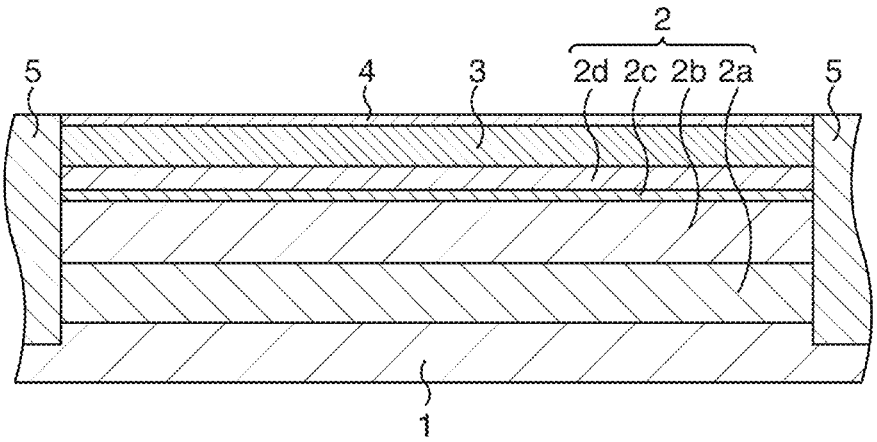


FIG. 2A

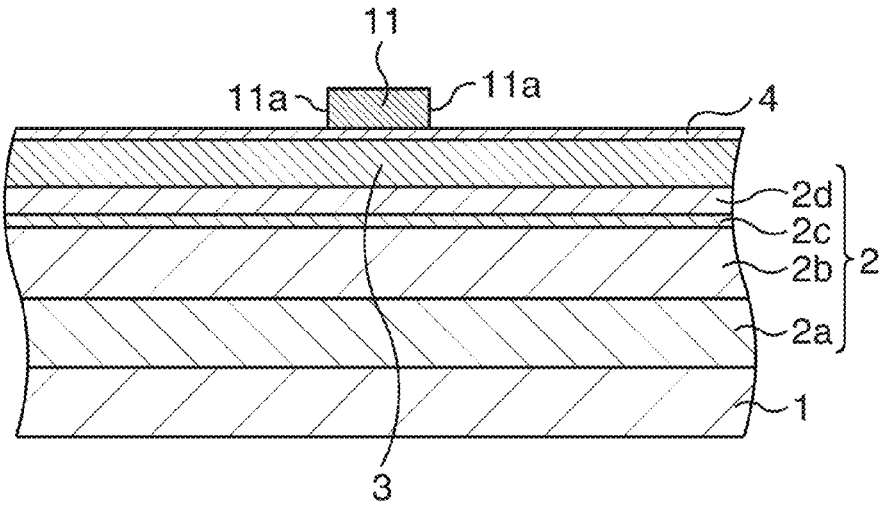

11
11a
11a
4
2d
2c
2b
2
2a
1
3

FIG. 2B

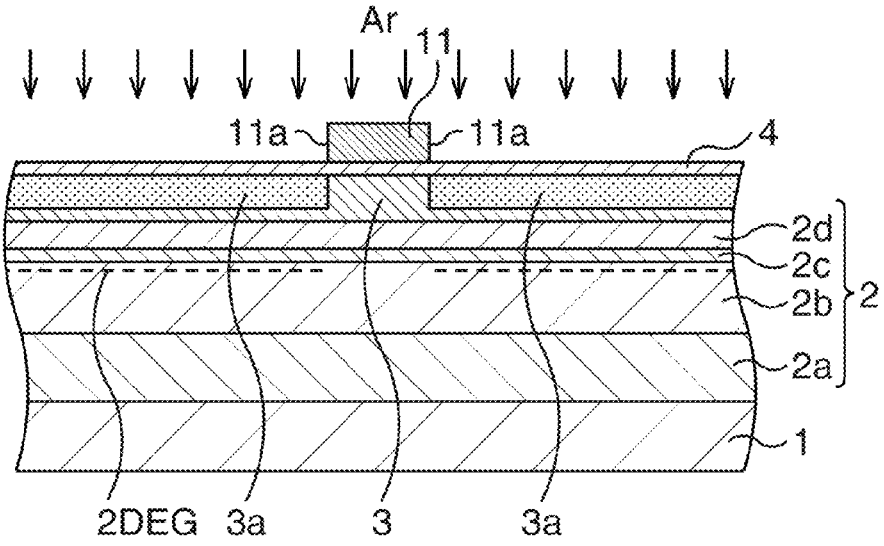

Ar
11
11a
11a
4
2d
2c
2b
2
2a
1
2DEG
3a
3
3a

FIG. 3A

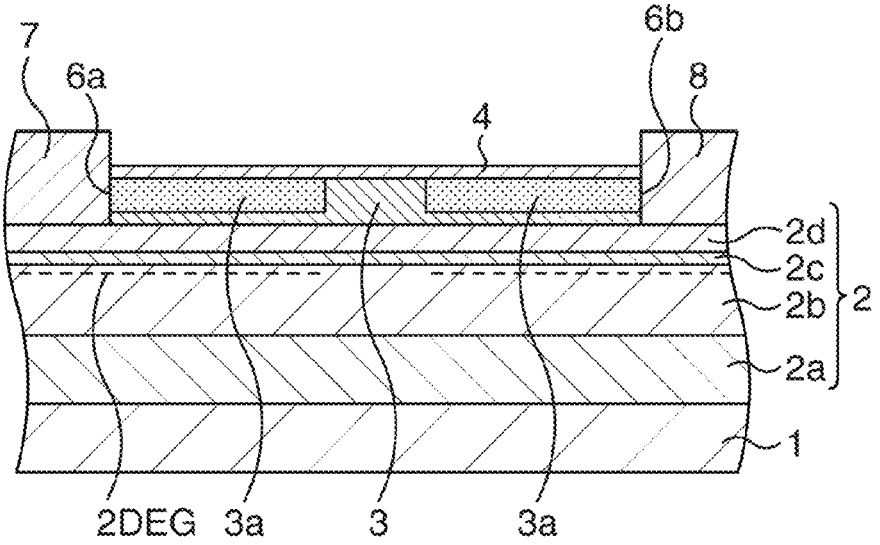

7
6a
6b
8
4
2d
2c
2b
2
2a
1
2DEG
3a
3
3a

FIG. 3B

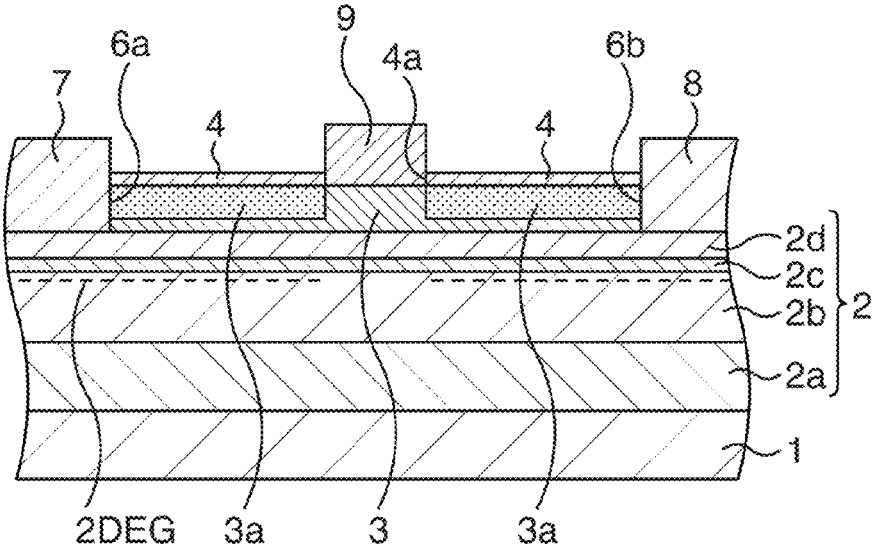

9
6a
4a
6b
7
8
4
4
2d
2c
2b
2
2a
1
2DEG
3a
3
3a

FIG. 4

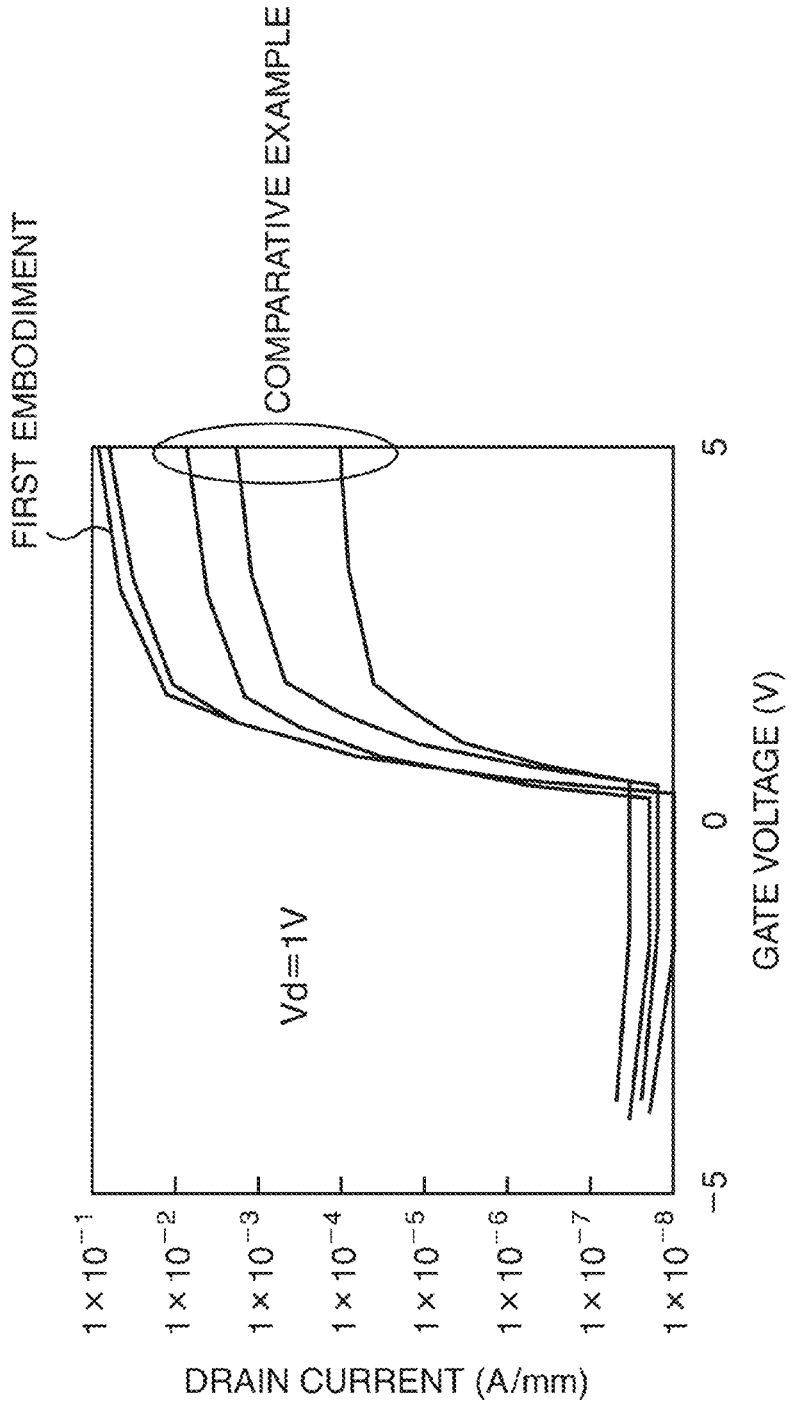

FIRST EMBODIMENT
COMPARATIVE EXAMPLE
Vd=1V
GATE VOLTAGE (V)
5
0
−5
DRAIN CURRENT (A/mm)
1×10⁻¹
1×10⁻²
1×10⁻³
1×10⁻⁴
1×10⁻⁵
1×10⁻⁶
1×10⁻⁷
1×10⁻⁸

FIG. 5A

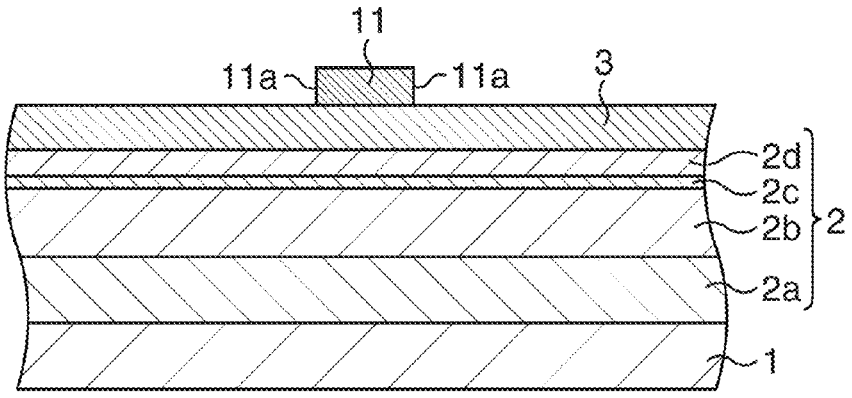


FIG. 5B

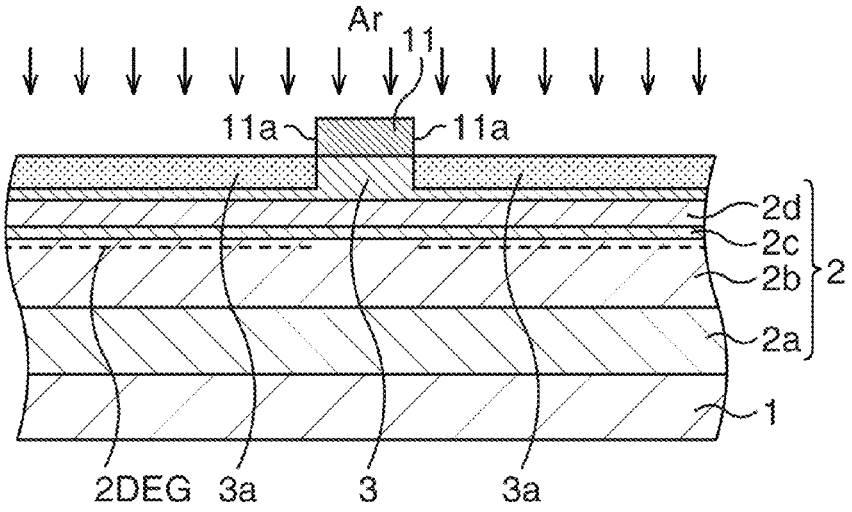


FIG. 6A

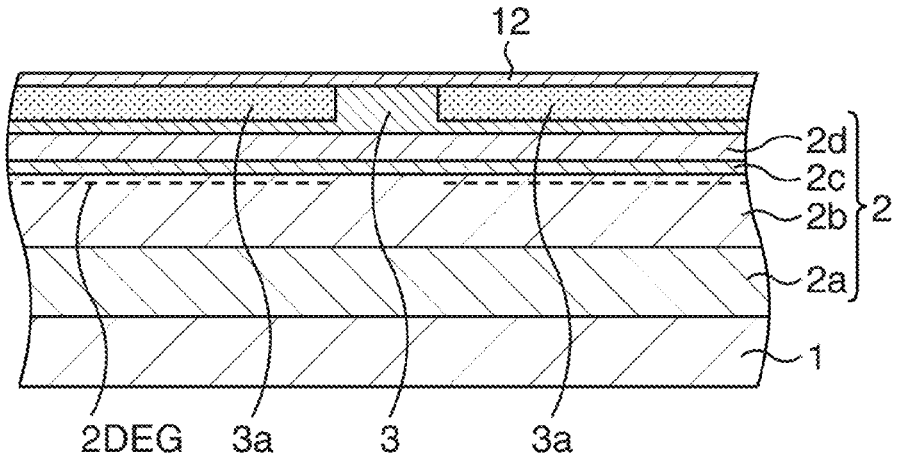

12
2d
2c
2b
2
2a
1
2DEG
3a
3
3a

FIG. 6B

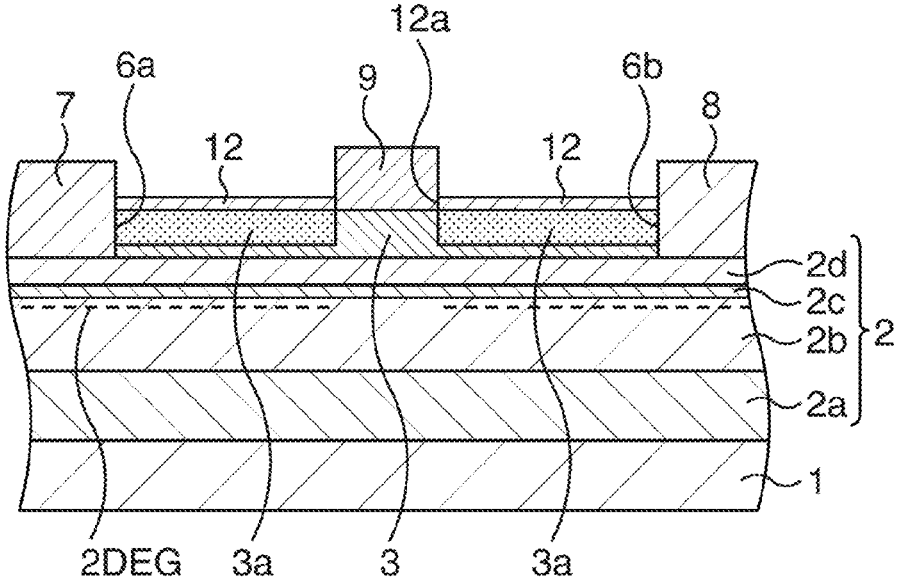

12a
6a
9
6b
7
8
12
12
2d
2c
2b
2
2a
1
2DEG
3a
3
3a

FIG. 7

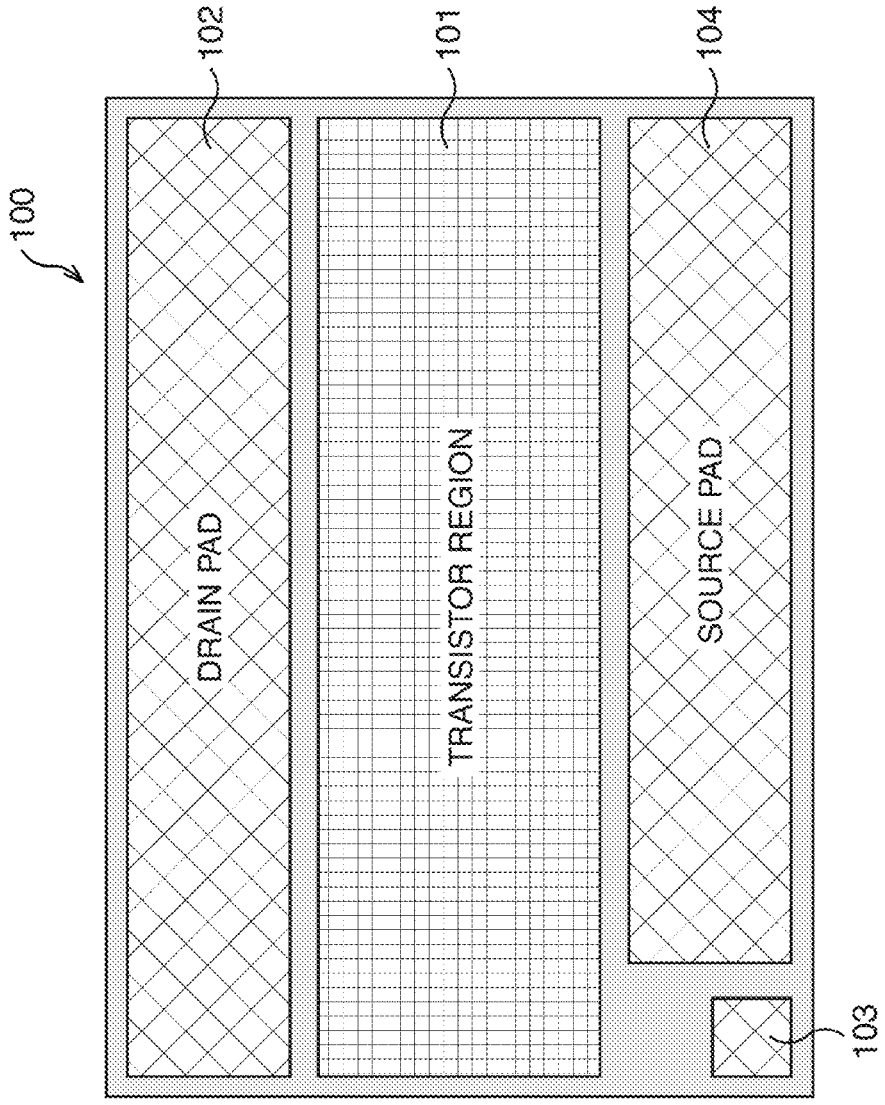


FIG. 8

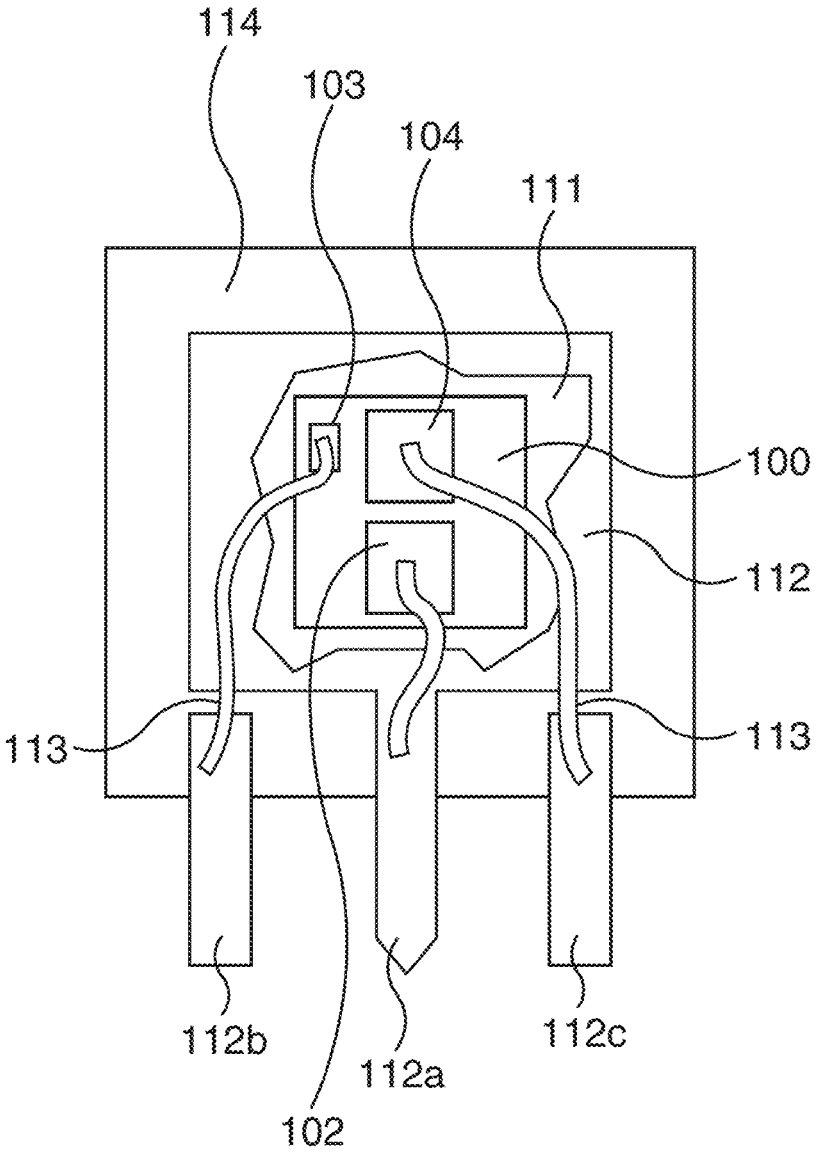


FIG. 9

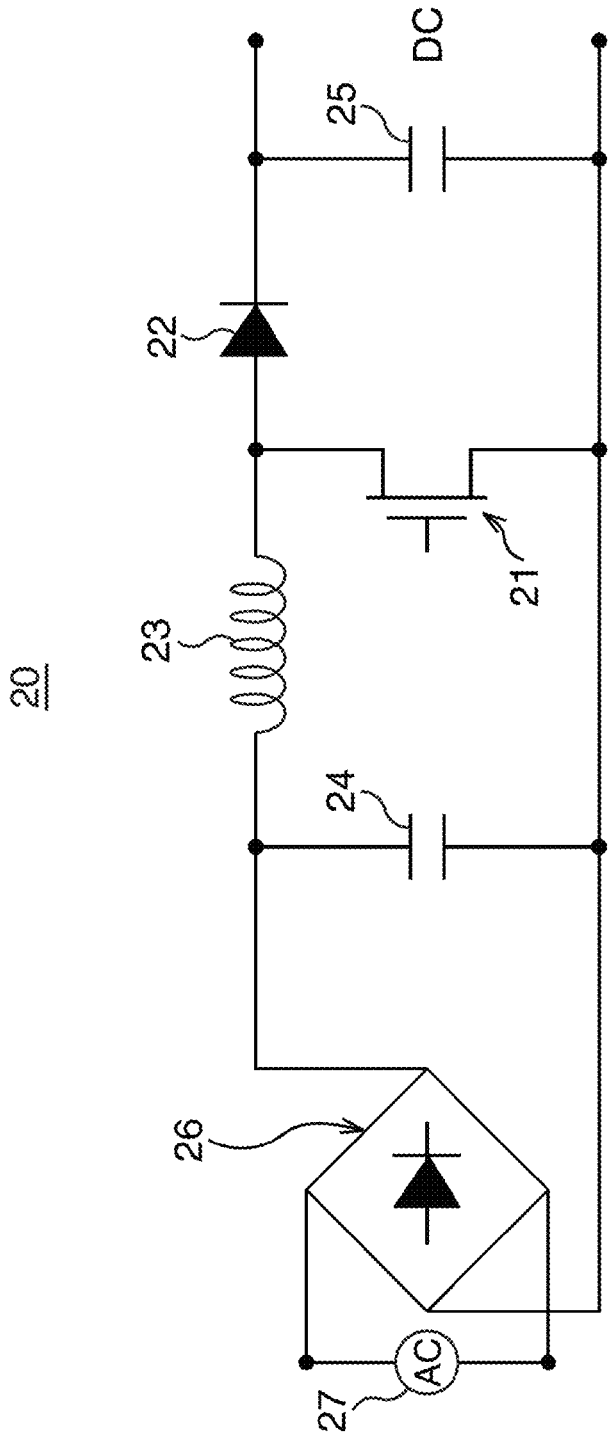


FIG. 10

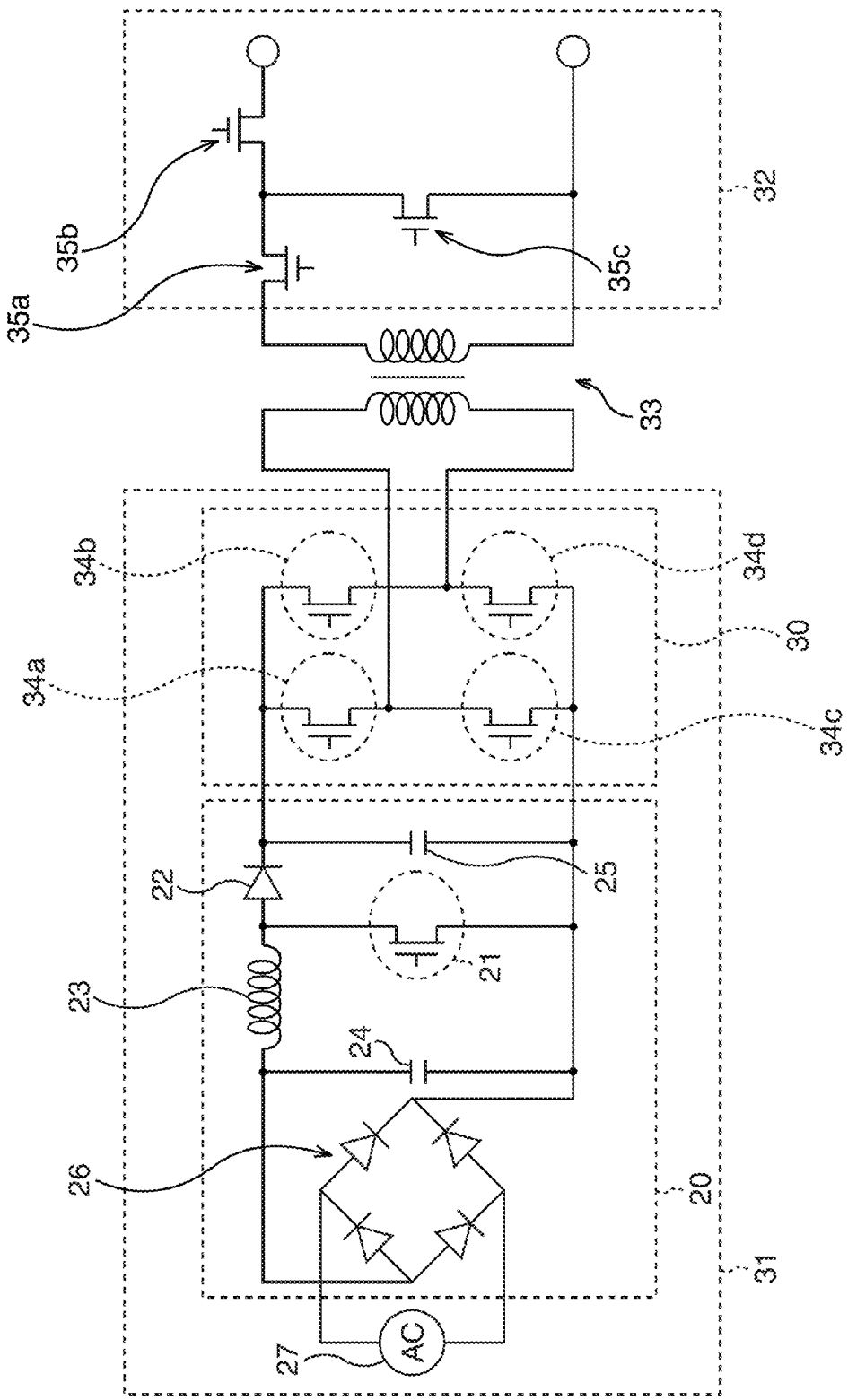
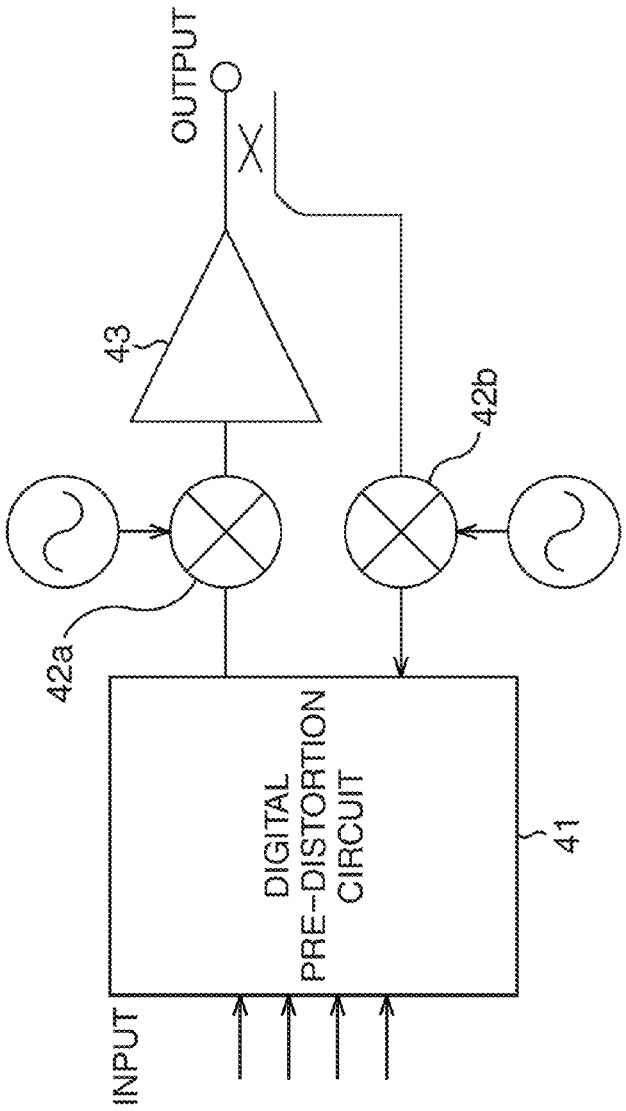


FIG. 11



COMPOUND SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD OF THE SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

This is a continuation of U.S. application Ser. No. 13/787,788, filed on Mar. 6, 2013, which is based upon and claims the benefit of priority of the prior Japanese Application No. 2012-077624, filed on Mar. 29, 2012. The disclosure of the prior applications are considered part of and are incorporated by reference in the disclosure of this application.

FIELD

The embodiments discussed herein are directed to a compound semiconductor device and a manufacturing method of the same.

BACKGROUND

A nitride semiconductor has been considered to be applied for a high withstand voltage and high-power semiconductor device by using characteristics such as high saturation electron velocity and wide band gap. For example, a band gap of GaN being the nitride semiconductor is 3.4 eV, and it is larger than a band gap of Si (1.1 eV) and a band gap of GaAs (1.4 eV), and has high breakdown electric field intensity. Accordingly, GaN is extremely expectable as a material of a semiconductor device for a power supply in high voltage operation and obtaining high-power.

As a device using the nitride semiconductor, a lot of reports have been made as for a field effect transistor, in particular, a high electron mobility transistor (HEMT). For example, in a GaN-based HEMT (GaN-HEMT), an AlGaN/GaN.HEMT in which GaN is used as an electron transit layer and AlGaN is used as an electron supply layer attracts attention. In the AlGaN/GaN.HEMT, a distortion resulting from a difference in lattice constants between GaN and AlGaN is generated at AlGaN. High-concentration two-dimensional electron gas (2DEG) is obtained by a piezoelectric polarization generated thereby and a spontaneous polarization of AlGaN. Therefore, it is expected as a high withstand electric power device such as a high-efficiency switch element and an electric vehicle.

[Patent Literature 1] Japanese Laid-open Patent Publication No. 2009-289827

[Patent Literature 2] Japanese Laid-open Patent Publication No. 2005-243727

In a nitride semiconductor device, an art locally controlling a generation amount of the 2DEG is required. For example, in case of the HEMT, it is desired that a current does not flow when a voltage is turned off, so-called a normally-off operation from so-called a fail-safe point of view. A device is necessary to suppress the generation amount of the 2DEG at downward of a gate electrode when the voltage is turned off to enable the above.

As one of methods enabling a GaN.HEMT performing the normally-off operation, a method is proposed in which a p-type GaN layer is formed on an electron supply layer, the 2DEG existing at a portion corresponding to beneath the p-type GaN layer is ceased to be directed to the normally-off operation. In this method, p-type GaN is grown at a whole surface of, for example, on AlGaN to be the electron supply layer, the p-type GaN is dry-etched to remain at a formation portion of the gate electrode to form a p-type GaN layer, and the gate electrode is formed thereon.

As stated above, the dry-etching is used for a patterning of the p-type GaN. A surface layer of the electron supply layer disposed under the p-type GaN is damaged by the dry-etching, as a result, a sheet resistance (R_{sh}) and a contact resistance (ρ_c) increase, and an on-resistance decrease. In this case, it is impossible to obtain an enough on-current (drain current) even though a gate voltage is applied. In addition, there is a problem in which a large variation occurs at the drain current.

SUMMARY

An aspect of a semiconductor device includes: a compound semiconductor lamination structure; a p-type semiconductor layer formed at upward of the compound semiconductor lamination structure; and an electrode formed at upward of the p-type semiconductor layer, wherein an inert element is introduced into both sides of the electrode, and introduced portions of the inert element are inactivated at the p-type semiconductor layer.

An aspect of a manufacturing method of a semiconductor device includes: forming a compound semiconductor lamination structure; forming a p-type semiconductor layer at an electrode formation region at upward of the compound semiconductor lamination structure; and inactivating an introduced portion of an inert element of the p-type semiconductor layer by introducing the inert element into both sides of the electrode formation region of the p-type semiconductor layer.

The object and advantages of the invention will be realized and attained by means of the elements and combinations particularly pointed out in the claims.

It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are not restrictive of the invention.

BRIEF DESCRIPTION OF DRAWINGS

FIG. **1**A to FIG. **1**C are schematic sectional views illustrating a manufacturing method of an AlGaN/GaN.HEMT according to a first embodiment in process sequence;

FIG. **2**A and FIG. **2**B are schematic sectional views illustrating the manufacturing method of the AlGaN/GaN.HEMT according to the first embodiment in process sequence subsequent to FIG. **1**A to FIG. **1**C;

FIG. **3**A and FIG. **3**B are schematic sectional views illustrating the manufacturing method of the AlGaN/GaN.HEMT according to the first embodiment in process sequence subsequent to FIG. **2**A and FIG. **2**B;

FIG. **4** is a characteristics chart representing a relationship between a gate voltage and a drain current at the AlGaN/GaN.HEMT;

FIG. **5**A and FIG. **5**B are schematic sectional views illustrating a manufacturing method of an AlGaN/GaN.HEMT according to a modification example of the first embodiment in process sequence;

FIG. **6**A and FIG. **6**B are schematic sectional views illustrating the manufacturing method of the AlGaN/GaN.HEMT according to the modification example of the first embodiment in process sequence subsequent to FIG. **5**A and FIG. **5**B;

FIG. **7** is a schematic plan view illustrating an HEMT chip using the AlGaN/GaN.HEMT according to the first embodiment or the modification example;

FIG. **8** is a schematic plan view illustrating a discrete package of the HEMT chip using the AlGaN/GaN.HEMT according to the first embodiment or the modification example;

FIG. **9** is a connection diagram illustrating a PFC circuit according to a second embodiment;

FIG. **10** is a connection diagram illustrating a schematic configuration of a power supply device according to a third embodiment; and

FIG. **11** is a connection diagram illustrating a schematic configuration of a high-frequency amplifier according to a fourth embodiment.

DESCRIPTION OF EMBODIMENTS

Hereinafter, preferred embodiments will be explained in detail with reference to accompanying drawings. In the following respective embodiments, a configuration of a compound semiconductor device is described together with a manufacturing method thereof.

Note that in the following drawings, there are components which are not illustrated as relatively accurate sizes and thicknesses as a matter of convenience of illustration.

First Embodiment

In the present embodiment, an AlGaN/GaN.HEMT is disclosed as a compound semiconductor device.

FIG. **1**A to FIG. **3**B are schematic sectional views illustrating a manufacturing method of an AlGaN/GaN.HEMT according to a first embodiment in process sequence.

At first, as illustrated in FIG. **1**A, a compound semiconductor lamination structure **2** and a p-type semiconductor layer **3** are formed on, for example, a semi-insulating Si substrate **1** as a growth substrate. A sapphire substrate, a GaAs substrate, a SiC substrate, a GaN substrate, and so on may be used as the growth substrate instead of the Si substrate. Besides, conductivity of the substrate is either semi-insulating or conductive.

The compound semiconductor lamination structure **2** is made up by including a nucleus formation layer **2***a*, an electron transit layer **2***b*, an intermediate layer (spacer layer) **2***c*, and an electron supply layer **2***d*. A p-type semiconductor layer **3** is formed on the electron supply layer **2***d*.

In detail, the following respective compound semiconductors are epitaxially grown on the Si substrate **1** by, for example, a metal organic vapor phase epitaxy (MOVPE) method. A molecular beam epitaxy (MBE) method, and so on may be used instead of the MOVPE method.

The respective compound semiconductors to be the nucleus formation layer **2***a*, the electron transit layer **2***b*, the intermediate layer (spacer layer) **2***c*, the electron supply layer **2***d*, and the p-type semiconductor layer **3** are sequentially grown on the Si substrate **1**. The nucleus formation layer **2***a* is formed by growing AlN for a thickness of, for example, approximately 0.1 μm on the Si substrate **1**. The electron transit layer **2***b* is formed by growing i(intentionally undoped)-GaN for a thickness of, for example, approximately 300 nm. The intermediate layer **2***c* is formed by growing i-AlGaN for a thickness of, for example, approximately 5 nm. The electron supply layer **2***d* is formed by growing n-AlGaN for a thickness of approximately 30 nm. The p-type semiconductor layer **3** is formed by growing p-GaN for, for example, approximately 30 nm. There is a case in which the intermediate layer **2***c* is not formed. The electron supply layer may be formed by forming i-AlGaN.

Mixed gas of trimethylgallium (TMGa) gas being a Ga source and ammonia (NH_3) gas is used as source gas for the growth of GaN. Mixed gas of trimethylaluminum (TMAl) gas, TMGa gas, and NH_3 gas is used as source gas for the growth of AlGaN. Presence/absence of supply of TMAl gas, TMGa gas, TMIn gas and flow rates thereof are appropriately set in accordance with the compound semiconductor layer to be grown. The flow rate of the NH_3 gas being a common source is set at approximately 100 sccm to 10 slm. Besides, a growth pressure is set at approximately 50 Torr to 300 Torr, and a growth temperature is set at approximately 800° C. to 1200° C.

When AlGaN is grown as an n-type, namely when the electron supply layer **2***d* (n-AlGaN) is formed, an n-type impurity is added to the source gas of AlGaN. Here, for example, silane (SiH_4) gas containing, for example, Si is added to the source gas at a predetermined flow rate to dope Si into AlGaN. A doping concentration of Si is set at approximately $1\times10^{18}/cm^3$ to $1\times10^{20}/cm^3$, for example, at approximately $1\times10^{18}/cm^3$.

When GaN is grown as a p-type, namely, when the p-type semiconductor layer **3** (p-GaN) is formed, a p-type impurity, for example, the one selected from Mg, C is added to the source gas of GaN. In the present embodiment, Mg is used as the p-type impurity. Mg is added to the source gas at a predetermined flow rate to dope Mg into GaN. A doping concentration of Mg is, for example, set at approximately $1\times10^{16}/cm^3$ to $1\times10^{21}/cm^3$. When the doping concentration is lower than approximately $1\times10^{16}/cm^3$, GaN does not fully become the p-type, and it becomes normally-on. When the doping concentration is higher than approximately $1\times10^{21}/cm^3$, crystallinity deteriorates, and enough characteristics cannot be obtained. Accordingly, the doping concentration of Mg is set at approximately $1\times10^{16}/cm^3$ to $1\times10^{21}/cm^3$, and thereby, it becomes the p-type semiconductor capable of obtaining enough characteristics. In the present embodiment, the doping concentration of Mg of the p-type semiconductor layer **3** is set at approximately $5\times10^{19}/cm^3$.

In a compound semiconductor lamination structure **2**, a piezoelectric polarization caused by the distortion resulting from a difference between a GaN lattice constant and an AlGaN lattice constant is generated at an interface between the electron transit layer **2***b* and the electron supply layer **2***d* (Accurately, an interface with the intermediate layer **2***c*. Hereinafter, it is referred to as a GaN/AlGaN interface) if the p-type semiconductor layer **3** is not formed. The 2DEG at high electron concentration is generated at a whole area of the GaN/AlGaN interface owing to both an effect of the piezoelectric polarization and an effect of a spontaneous polarization of the electron transit layer **2***b* and the electron supply layer **2***d*.

The p-type semiconductor layer **3** is formed on the compound semiconductor lamination structure **2**, and thereby, the 2DEG at the GaN/AlGaN interface is ceased and disappeared. In FIG. **1**A, an appearance in which the 2DEG is disappeared is illustrated.

Subsequently, a protective insulating film **4** is formed as illustrated in FIG. **1**B.

In detail, an insulating film, for example, a silicon nitride film (SiN film) is deposited on the p-type semiconductor layer **3** to cover it for, for example, a film thickness of approximately 40 nm by a plasma CVD method and so on. The protective insulating film **4** covering on the p-type semiconductor layer **3** is thereby formed. For example, a silicon oxide film (SiO_2 film) and so on may be deposited as the protective insulating film.

Subsequently, an element isolation structure **5** is formed as illustrated in FIG. **1**C. The element isolation structure **5** is not illustrated in FIG. **2**A and later.

In detail, for example, argon (Ar) is injected into an element isolation region of the compound semiconductor lamination structure **2**. The element isolation structure **5** is thereby

formed at the compound semiconductor lamination structure **2**. An active region is defined on the compound semiconductor lamination structure **2** by the element isolation structure **5**.

Note that the element isolation may be performed by using the other already known methods such as, for example, an STI (Shallow Trench Isolation) method instead of the above-stated injection method. At this time, for example, chlorine etching gas is used for the dry-etching of the compound semiconductor lamination structure **2**.

Subsequently, a resist mask **11** is formed on the protective insulating film **4** as illustrated in FIG. **2**A.

In detail, a resist is coated on the protective insulating film **4**, the resist is processed by lithography, and the resist mask **11** opening at portions corresponding to both sides of a formation planned portion of a gate electrode of the protective insulating film **4** is formed. The openings of the resist mask **11** are set to be openings **11***a*.

Subsequently, an inert element is introduced into the p-type semiconductor layer **3** as illustrated in FIG. **2**B.

In detail, the inert element inactivating p-GaN is injected into the p-type semiconductor layer **3** by using the resist mask **11**. For example, argon (Ar), iron (Fe), phosphorus (P), oxygen (O_2) or boron (B) or any combination thereof, here, Ar is used as the inert element. For example, Ar is injected under a condition of an acceleration energy at approximately 10 keV, and a dose amount at approximately $1\times10^{14}/cm^2$. Ar passes through portions of the protective insulating film **4** exposed by the openings **11***a*, and Ar is introduced into only the p-type semiconductor layer **3** at downward of the opening portions by the resist mask **11**. Ar is introduced with the above-stated injection conditions, and thereby, Ar is introduced into surface layer portions of the p-type semiconductor layer, and non-introduced portions of Ar remain at downward of the surface layer portions. The surface layer portions of the p-type semiconductor layer **3** into which Ar is introduced are set to be Ar introduced regions **3***a*. The Ar introduced regions **3***a* are formed as stated above, and thereby, Ar remains at the surface layer portion, does not reach the electron supply layer **2***d*, and damages of the electron supply layer **2***d* caused by the injection of Ar is prevented.

The resist mask **11** is removed by an asking process, a chemical solution treatment, or the like.

Ar being the inert element inactivating p-GaN is injected into the p-type semiconductor layer **3**, and thereby, the 2DEG appears again at portions positionally matching with the portions at downward of the Ar introduced regions **3***a* at the GaN/AlGaN interface. It is thereby possible to secure high-concentration 2DEG at a necessary portion, to effectively cease the 2DEG only at a portion positionally matching with the formation planned portion of the gate electrode, and a certain normally-off is enabled.

It is possible to use the cited substances in the above, for example, Fe instead of Ar as the inert element. Fe is a relatively heavy element, and it is possible to surely inactivate only the surface layer portion of the p-type semiconductor layer **3** with low acceleration energy.

Subsequently, a source electrode **7** and a drain electrode **8** are formed as illustrated in FIG. **3**A.

In detail, at first, electrode recesses **6***a*, **6***b* are formed at formation planned portions of the source electrode and the drain electrode.

A resist is coated on a surface of the compound semiconductor lamination structure **2**. The resist is processed by lithography to form openings exposing surfaces of the protective insulating film **4** corresponding to the formation planned portions of the source electrode and the drain electrode. The resist mask having the openings is thereby formed at the resist.

The formation planned portions of the source electrode and the drain electrode of the protective insulating film **4** and the p-type semiconductor layer **3** are removed by dry-etching until a surface of the electron supply layer **2***d* exposes by using this resist mask. The electrode recesses **6***a*, **6***b* exposing the formation planned potions of the source electrode and the drain electrode of the surface of the electron supply layer **2***d* are thereby formed. As etching conditions, inert gas such as Ar and chlorine gas such as Cl_2 are used as etching gas, and for example, it is set that a flow rate of Cl_2 is 30 sccm, a pressure is 2 Pa, and an RF input power is 20 W. Note that the electrode recesses **6***a*, **6***b* may be formed by etching deeper than the surface of the electron supply layer **2***d*.

The resist mask is removed by the asking process, the chemical solution treatment, or the like.

A resist mask to form the source electrode and the drain electrode is formed. Here, for example, a two-layer resist in eaves structure suitable for a vapor deposition method and a lift-off method is used. This resist is coated on the compound semiconductor lamination structure **2**, and openings exposing the electrode recesses **6***a*, **6***b* are formed. The resist mask having the openings is thereby formed.

For example, Ta/Al is deposited as an electrode material on the resist mask including inside of the openings exposing the electrode recesses **6***a*, **6***b* by, for example, the vapor deposition method by using the resist mask. A thickness of Ta is approximately 30 nm, and a thickness of Al is approximately 200 nm. The resist mask and Ta/Al deposited thereon are removed by the lift-off method. After that, the Si substrate **1** is heat processed in, for example, nitrogen atmosphere, at a temperature of approximately 400° C. to 1000° C., for example, at approximately 600° C., and the remaining Ta/Al is brought into ohmic contact with the electron supply layer **2***d*. There is a case when the heat process is not necessary as long as the ohmic contact of Ta/Al with the electron supply layer **2***d* is obtained. The source electrode **7** and the drain electrode **8** in which the electrode recesses **6***a*, **6***b* are embedded by a part of the electrode material are thereby formed.

Subsequently, a gate electrode **9** is formed as illustrated in FIG. **3**B.

In detail, at first, an electrode recess **6***c* is formed at a formation planned portion of the gate electrode.

A resist is coated on the surface of the compound semiconductor lamination structure **2**. The resist is processed by lithography to form an opening exposing the surface of the protective insulating film **4** corresponding to the formation planned portion of the gate electrode at the resist. The resist mask having the opening is thereby formed.

The formation planned portion of the protective insulating film **4** is dry-etched to be removed until the surface of the p-type semiconductor layer **3** exposes by using this resist mask. An electrode recess **4***a* exposing the formation planned portion of the gate electrode at the surface of the p-type semiconductor layer **3** is thereby formed at the protective insulating film **4**. As etching conditions thereof, the inert gas such as Ar and the chlorine gas such as Cl_2 are used as the etching gas, and for example, it is set that the flow rate of Cl_2 is 30 sccm, the pressure is 2 Pa, and the RF input power is 20 W.

The resist mask is removed by the asking process, the chemical solution treatment, or the like.

A resist mask to form the gate electrode is formed. Here, for example, the two-layer resist in eaves structure suitable for the vapor deposition method and the lift-off method is

used. This resist is coated on the compound semiconductor lamination structure **2**, and an opening exposing the electrode recess **4***a* being the formation planned portion of the gate electrode of the p-type semiconductor layer **3** is formed. The resist mask having the opening is thereby formed.

For example, Ni/Au is deposited as the electrode material on the resist mask including inside of the electrode recess **4***a* exposed by the opening by, for example, the vapor deposition method by using the resist mask. A thickness of Ni is approximately 30 nm, and a thickness of Au is approximately 400 nm. The resist mask and Ni/Au deposited thereon are removed by the lift-off method. The gate electrode **9** is thereby formed on a portion between the Ar introduced regions **3***a* at the p-type semiconductor layer **3**. The gate electrode **9** is brought into Schottky contact with the p-type semiconductor layer **3**.

Note that the protective insulating film **4** is used as a gate insulating film, and therefore, the gate electrode **9** may be formed on the p-type semiconductor layer **3** via the protective insulating film **4** without forming the electrode recess **4***a* at the protective insulating film **4**. In this case, an MIS type AlGaN/GaN.HEMT is formed.

After that, the AlGaN/GaN.HEMT according to the present embodiment is formed by going through respective processes such as formation of wirings to be connected to the source electrode **7**, the drain electrode **8**, and the gate electrode **9**.

A relationship between a gate voltage and a drain current is investigated as for the AlGaN/GaN.HEMT according to the present embodiment based on a comparison with an AlGaN/GaN.HEMT according to a comparative example. The result thereof is represented in FIG. **4**. In the AlGaN/GaN.HEMT according to the comparative example, the introduction of the inert element according to the present embodiment is not performed, and a gate electrode is formed on a p-type semiconductor layer patterned by dry-etching. Plural samples of the manufactured AlGaN/GaN.HEMTs are studied as objects as for both the present embodiment and the comparative example.

As represented in FIG. **4**, it is verified that values of the drain currents are low and a large variation occurs in the drain currents by each sample in the comparative example. On the other hand, the values of the drain currents are higher than the comparative example, and the variation seldom occurs in the drain currents by each sample in the present embodiment.

In the AlGaN/GaN.HEMTs according to the comparative example, AlGaN of the electron supply layer is largely damaged by the dry-etching of the p-type semiconductor layer, and thereby, the drain current extremely decreases. Besides, a control of the dry-etching of the p-type semiconductor layer is difficult, and etching states (for example, etching amounts of AlGaN of the electron supply layer) are different by each product, and thereby, the variation of the drain currents occurs.

In the AlGaN/GaN.HEMT according to the present embodiment, only the necessary 2DEG is resumed by injecting the inert element without performing the dry-etching of the p-type semiconductor layer. In the injection of the inert element, it is possible to accurately inject the inert element at a desired concentration into a desired region. Accordingly, it is possible to perform the injection of the inert element without damaging AlGaN of the electron supply layer and without any variation by each product. It is thereby possible to obtain the AlGaN/GaN.HEMT of which value of the drain current is high and without almost any variation in the drain current in the present embodiment.

As stated above, the AlGaN/GaN.HEMT with high reliability in which the device characteristics are improved by securing the stable and large drain current without any variation, and the certain normally-off is enabled is enabled in the present embodiment.

Modification Example

Hereinafter, a modification example of the first embodiment is described. In the modification example, an AlGaN/GaN.HEMT similar to the first embodiment is disclosed, but it is different from the first embodiment in a point in which a manufacturing method thereof is partly different.

FIGS. **5**A, **5**B and FIGS. **6**A, **6**B are schematic sectional views illustrating main processes in a manufacturing method of the AlGaN/GaN.HEMT according to the modification example of the first embodiment. Note that the same reference numerals are used to designate similar components and so on as the first embodiment, and detailed description thereof is not given.

In the modification example, at first, the element isolation structure **5** is formed by the process of FIG. **1**C after the compound semiconductor lamination structure **2** and the p-type semiconductor layer **3** are formed by the process of FIG. **1**A of the first embodiment.

Subsequently, the resist mask **11** is formed on the p-type semiconductor layer **3** as illustrated in FIG. **5**A.

In detail, the resist is coated on the p-type semiconductor layer **3**, the resist is processed by lithography, and the resist mask **11** opening at portions corresponding to both sides of the formation planned portion of the gate electrode of the p-type semiconductor layer **3** is formed. The openings of the resist mask **11** are set to be the openings **11***a*.

Subsequently, the inert element is introduced into the p-type semiconductor layer **3** as illustrated in FIG. **5**B.

In detail, the inert element inactivating p-GaN is directly injected into the p-type semiconductor layer **3** by using the resist mask **11**. For example, argon (Ar), iron (Fe), phosphorus (P), oxygen (O_2) or boron (B) or any combination thereof, here, Ar is used as the inert element. For example, Ar is injected under a condition of an acceleration energy at approximately 15 keV, and a dose amount at approximately $1\times10^{14}/cm^2$. Ar is introduced into only at portions of the p-type semiconductor layer **3** exposed by the openings **11***a* by the resist mask **11**. Ar is introduced with the above-stated injection conditions, and thereby, Ar is introduced into the surface layer portions of the p-type semiconductor layer, and the non-introduced portions of Ar remain at downward of the surface layer portions. The surface layer portions of the p-type semiconductor layer **3** into which Ar is introduced are set to be the Ar introduced regions **3***a*. The Ar introduced regions **3***a* are formed as stated above, and thereby, Ar remains at the surface layer portion, does not reach the electron supply layer **2***d*, and damages of the electron supply layer **2***d* caused by the injection of Ar is prevented.

The resist mask **11** is removed by the asking process, the chemical solution treatment, or the like.

Ar being the inert element inactivating p-GaN is injected into the p-type semiconductor layer **3**, and thereby, the 2DEG appears again at the portions positionally matching with the portions at downward of the Ar introduced regions **3***a* at the GaN/AlGaN interface. It is thereby possible to secure the high-concentration 2DEG at the necessary portion, and to effectively cease the 2DEG only at the portion positionally matching with the formation planned portion of the gate electrode, and thereby, the certain normally-off is enabled.

It is possible to use the cited substances in the above, for example, Fe instead of Ar as the inert element. Fe is the relatively heavy element, and it is possible to surely inactivate

only the surface layer portion of the p-type semiconductor layer **3** with low acceleration energy.

The resist mask **11** is removed by the asking process, the chemical solution treatment, or the like.

Subsequently, a protective insulting film **12** is formed as illustrated in FIG. **6**A.

In detail, an insulating film, for example, a silicon nitride film (SiN film) is deposited on the p-type semiconductor layer **3** to cover it for, for example, a film thickness of approximately 40 nm by a plasma CVD method and so on. The protective insulating film **12** covering the p-type semiconductor layer **3** is thereby formed. As the protective insulating film, for example, a silicon oxide film (SiO_2 film) and so on may be deposited.

After that, the source electrode **7**, the drain electrode **8**, and the gate electrode **9** are formed as illustrated in FIG. **6**B by performing the processes in FIG. **3**A and FIG. **3**B.

Note that the protective insulating film **12** is used as a gate insulating film, and therefore, the gate electrode **9** may be formed on the p-type semiconductor layer **3** via the protective insulating film **12** without forming the electrode recess at the protective insulating film **12**. In this case, the MIS type AlGaN/GaN.HEMT is formed.

After that, the AlGaN/GaN.HEMT according to the modification example is formed by going through respective processes such as formation of wirings to be connected to the source electrode **7**, the drain electrode **8**, and the gate electrode **9**.

In the modification example, the AlGaN/GaN.HEMT with high reliability is enabled in which the device characteristics are improved by securing the stable and large drain current without any variation, and the certain normally-off is enabled.

The AlGaN/GaN.HEMT according to the first embodiment or the modification example is applied to so-called a discrete package.

In this discrete package, a chip of the AlGaN/GaN.HEMT according to the first embodiment or the modification example is mounted. Hereinafter, the discrete package of the chip of the AlGaN/GaN.HEMT according to the first embodiment or the modification example (hereinafter, referred to as an HEMT chip) is exemplified.

A schematic configuration of the HEMT chip is illustrated in FIG. **7**.

In an HEMT chip **100**, a transistor region **101** of the AlGaN/GaN.HEMT, a drain pad **102** to which the drain electrode is connected, a gate pad **103** to which the gate electrode is connected, and a source pad **104** to which the source electrode is connected are provided at a surface thereof.

FIG. **8** is a schematic plan view illustrating the discrete package.

At first, the HEMT chip **100** is fixed to a lead frame **112** by using a die attach agent **111** such as a solder to manufacture the discrete package. A drain lead **112***a* is integrally formed at the lead frame **112**, and a gate lead **112***b* and a source lead **112***c* are disposed apart from the lead frame **112** as individual bodies.

Subsequently, the drain pad **102** and the drain lead **112***a*, the gate pad **103** and the gate lead **112***b*, and the source pad **104** and the source lead **112***c* are each electrically connected by a bonding using Al wires **113**.

After that, the HEMT chip **100** is resin-sealed by a transfer molding method by using a molding resin **114**, and the lead frame **112** is detached. The discrete package is thereby formed.

Second Embodiment

In the present embodiment, a PFC (Power Factor Correction) circuit including the AlGaN/GaN.HEMT according to one kind selected from the first embodiment and the modification example is disclosed.

FIG. **9** is a connection diagram illustrating the PFC circuit.

A PFC circuit **20** is made up by including a switch element (transistor) **21**, a diode **22**, a choke coil **23**, capacitors **24**, **25**, a diode bridge **26**, and an alternating-current power supply (AC) **27**. The AlGaN/GaN.HEMT according to one kind selected from the first embodiment and the modification example is applied for the switch element **21**.

In the PFC circuit **20**, a drain electrode of the switch element **21**, an anode terminal of the diode **22** and one terminal of the choke coil **23** are connected. A source electrode of the switch element **21**, one terminal of the capacitor **24** and one terminal of the capacitor **25** are connected. The other terminal of the capacitor **24** and the other terminal of the choke coil **23** are connected. The other terminal of the capacitor **25** and a cathode terminal of the diode **22** are connected. The AC **27** is connected between both terminals of the capacitor **24** via the diode bridge **26**. A direct-current power supply (DC) is connected between both terminals of the capacitor **25**. Note that a not-illustrated PFC controller is connected to the switch element **21**.

In the present embodiment, the AlGaN/GaN.HEMT according to one kind selected from the first embodiment and the modification example is applied for the PFC circuit **20**. A high reliability PFC circuit **20** is thereby enabled.

Third Embodiment

In the present embodiment, a power supply device including the AlGaN/GaN.HEMT according to one kind selected from the first embodiment and the modification example is disclosed.

FIG. **10** is a connection diagram illustrating a schematic configuration of the power supply device according to a third embodiment.

The power supply device according to the present embodiment is made up by including a high-pressure primary side circuit **31**, a low-pressure secondary side circuit **32**, and a transformer **33** disposed between the primary side circuit **31** and the secondary side circuit **32**.

The primary side circuit **31** includes the PFC circuit **20** according to the second embodiment, and an inverter circuit connected between the both terminals of the capacitor **25** of the PFC circuit **20**, for example, a full-bridge inverter circuit **30**. The full-bridge inverter circuit **30** is made up by including plural (here, four pieces of) switch elements **34***a*, **34***b*, **34***c*, and **34***d*.

The secondary side circuit **32** is made up by including plural (here, three pieces of) switch elements **35***a*, **35***b*, and **35***c*.

In the present embodiment, the PCF circuit constituting the primary side circuit **31** is the PFC circuit **20** according to the second embodiment, and the switch elements **34***a*, **34***b*, **34***c*, and **34***d* of the full-bridge inverter circuit **30** are the AlGaN/GaN.HEMTs according to one kind selected from the first embodiment and the modification example. On the other hand, the switch elements **35***a*, **35***b*, and **35***c* of the secondary side circuit **32** are normal MIS.FETs using silicon.

In the present embodiment, the PFC circuit **20** according to the second embodiment and the AlGaN/GaN.HEMTs according to one kind selected from the first embodiment or the modification example are applied for the primary side

circuit **31** being the high-pressure circuit. A high-reliability and high-power power supply device is thereby enabled.

Fourth Embodiment

In the present embodiment, a high-frequency amplifier including the AlGaN/GaN.HEMT according to one kind selected from the first embodiment and the modification example is disclosed.

FIG. **11** is a connection diagram illustrating a schematic configuration of the high-frequency amplifier according to a fourth embodiment.

The high-frequency amplifier according to the present embodiment is made up by including a digital pre-distortion circuit **41**, mixers **42***a*, **42***b*, and a power amplifier **43**.

The digital pre-distortion circuit **41** is to compensate a nonlinear distortion of an input signal. The mixer **42***a* is to mix the input signal of which nonlinear distortion is compensated with an AC signal. The power amplifier **43** is to amplify the input signal mixed with the AC signal, and includes the AlGaN/GaN.HEMT according to one kind selected from the first embodiment and the modification example. Note that in FIG. **11**, it is constituted such that a signal at an output side is able to be mixed with the AC signal by the mixer **42***b* and to transmit to the digital pre-distortion circuit **41** by, for example, a switching of a switch.

In the present embodiment, the AlGaN/GaN.HEMT according to one kind selected from the first embodiment and the modification example is applied for the high-frequency amplifier. The high reliability, high withstand voltage, and high-frequency amplifier is thereby enabled.

Other Embodiments

In the first embodiment and the modification example, the AlGaN/GaN.HEMT is exemplified as the compound semiconductor device. It is applicable for the following HEMTs other than the AlGaN/GaN.HEMT as the compound semiconductor device.

The Other Device Example 1

In the present example, an InAlN/GaN.HEMT is disclosed as the compound semiconductor device.

InAlN and GaN are compound semiconductors capable of approximating lattice constants by compositions thereof. In this case, the electron transit layer is formed by i-GaN, the intermediate layer is formed by AlN, the electron supply layer is formed by n-InAlN, and the p-type semiconductor layer is formed by p-GaN in the first embodiment and the modification example. Besides, the piezoelectric polarization is seldom generated in this case, and therefore, the two-dimensional electron gas is mainly generated by the spontaneous polarization of InAlN.

According to the present example, a high reliability InAlN/GaN.HEMT improving the device characteristics by securing the stable and large drain current without any variation, and enabling the certain normally-off is enabled as same as the above-stated AlGaN/GaN.HEMT.

The Other Device Example 2

In the present example, an InAlGaN/GaN.HEMT is disclosed as the compound semiconductor device.

GaN and InAlGaN are compound semiconductors capable of making the lattice constant of the latter one smaller than the former one by compositions thereof. In this case, the electron transit layer is formed by i-GaN, the intermediate layer is formed by i-InAlGaN, the electron supply layer is formed by n-InAlGaN, and the p-type semiconductor layer is formed by p-GaN in the first embodiment and the modification example.

According to the present example, a high reliability InAlGaN/GaN.HEMT improving the device characteristics by securing the stable and large drain current without any variation, and enabling the certain normally-off is enabled as same as the above-stated AlGaN/GaN.HEMT.

According to each aspect, a high reliability compound semiconductor device improving device characteristics by securing a stable and large drain current without any variation, and enabling a certain normally-off is enabled.

All examples and conditional language provided herein are intended for the pedagogical purposes of aiding the reader in understanding the invention and the concepts contributed by the inventor to further the art, and are not to be construed as limitations to such specifically recited examples and conditions, nor does the organization of such examples in the specification relate to a showing of the superiority and inferiority of the invention. Although one or more embodiments of the present invention have been described in detail, it should be understood that the various changes, substitutions, and alterations could be made hereto without departing from the spirit and scope of the invention.

What is claimed is:

1. A compound semiconductor device, comprising:

a compound semiconductor lamination structure including a nitride semiconductor;

a p-type nitride semiconductor layer formed upward of the compound semiconductor lamination structure; and

a gate electrode formed upward of the p-type nitride semiconductor layer,

wherein the p-type nitride semiconductor layer includes portions on opposite sides of the gate electrode in which inert elements have been introduced, the inert elements causing the portions of the p-type nitride semiconductor layer to be inactivated, and resulting in the presence of a two-dimensional electron gas in regions of the compound semiconductor lamination structure that are below the portions of the p-type nitride semiconductor layer on opposite sides of the gate electrode but not in a region of the compound semiconductor lamination structure that is below the gate electrode.

2. The compound semiconductor device according to claim **1**, wherein the nitride semiconductor includes a layer of GaN and a layer of AlGaN, and the two-dimensional electron gas is in the layer of GaN.

3. The compound semiconductor device according to claim **2**, wherein the nitride semiconductor further includes a layer of AlN between the layer of GaN and the layer of AlGaN.

4. The compound semiconductor device according to claim **1**, further comprising a protective insulating film that covers the portions of the p-type nitride semiconductor layer on opposite sides of the gate electrode.

5. The compound semiconductor device according to claim **1**, wherein the inert elements comprise argon (Ar), iron (Fe), phosphorus (P), oxygen (O_2) or boron (B) or any combination thereof.

6. The compound semiconductor device according to claim **1**, wherein the p-type nitride semiconductor layer comprises GaN.

7. The compound semiconductor device according to claim **1**, wherein the device comprises a source electrode and a drain electrode on opposite sides of the gate electrode, and the

portions of the p-type nitride semiconductor layer containing the inert element each extend from the gate electrode to the source or drain electrode.

8. A method of manufacturing a compound semiconductor device, comprising:

forming a compound semiconductor lamination structure which includes a nitride semiconductor;

forming a p-type nitride semiconductor layer upward of the compound semiconductor lamination structure;

forming a gate electrode upward of the p-type semiconductor layer; and

introducing inert elements into portions of the p-type nitride semiconductor layer on opposite sides of the gate electrode, thereby causing the portions of the p-type nitride semiconductor layer to be inactivated and resulting in the presence of a two-dimensional electron gas in regions of the compound semiconductor lamination structure that are below the portions of the p-type nitride semiconductor layer but not in a region of the compound semiconductor lamination structure that is directly below the gate electrode.

9. The method of manufacturing the compound semiconductor device according to claim **8**, wherein the nitride semiconductor includes a layer of GaN and a layer of AlGaN, and the two-dimensional electron gas is in the layer of GaN.

10. The method of manufacturing the compound semiconductor device according to claim **9**, wherein the nitride semiconductor further includes a layer of AlN between the layer of GaN and the layer of AlGaN.

11. The method of manufacturing the compound semiconductor device according to claim **8**, further comprising forming a protective insulating film on the p-type nitride semiconductor layer, wherein the inert elements are introduced into the p-type nitride semiconductor layer through the protective insulating film.

12. The method of manufacturing the compound semiconductor device according to claim **8**, further comprising forming a protective insulating film that covers the portions of the p-type nitride semiconductor layer on opposite sides of the gate electrode after the introducing of the inert elements into the p-type nitride semiconductor layer.

13. The method of manufacturing the compound semiconductor device according to claim **8**, wherein the inert elements comprise argon (Ar), iron (Fe), phosphorus (P), oxygen (O_2) or boron (B) or any combination thereof.

14. The method of manufacturing the compound semiconductor device according to claim **8**, further comprising forming a source electrode and a drain electrode on opposite sides of the gate electrode, wherein the portions of the p-type nitride semiconductor layer containing the inert element each extend from the gate electrode to the source or drain electrode.

15. A power supply device, comprising:

a transformer;

a high-pressure circuit and a low-pressure circuit that sandwich the transformer therebetween,

wherein the high-pressure circuit includes a transistor, and the transistor includes:

a compound semiconductor lamination structure which includes a nitride semiconductor;

a p-type nitride semiconductor layer formed upward of the compound semiconductor lamination structure; and

a gate electrode formed upward of the p-type nitride semiconductor layer,

wherein the p-type nitride semiconductor layer includes portions on opposite sides of the gate electrode in which inert elements have been introduced, the inert elements causing the portions of the p-type nitride semiconductor layer to be inactivated, and resulting in the presence of a two-dimensional electron gas in regions of the compound semiconductor lamination structure that are below the portions of the p-type nitride semiconductor layer on opposite sides of the gate electrode but not in a region of the compound semiconductor lamination structure that is below the gate electrode.

16. The power supply device according to claim **15**, wherein the nitride semiconductor includes a layer of GaN and a layer of AlGaN, and the two-dimensional electron gas is in the layer of GaN.

17. The power supply device according to claim **16**, wherein the nitride semiconductor further includes a layer of AlN between the layer of GaN and the layer of AlGaN.

18. The power supply device according to claim **15**, further comprising a protective insulating film that covers the portions of the p-type nitride semiconductor layer on opposite sides of the gate electrode.

19. The power supply device according to claim **15**, wherein the p-type nitride semiconductor layer comprises GaN.

20. The power supply device according to claim **15**, wherein the transistor further includes a source electrode and a drain electrode on opposite sides of the gate electrode, and the portions of the p-type nitride semiconductor layer containing the inert element each extend from the gate electrode to the source or drain electrode.

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